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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,945	08/10/2000	Setsuo Nakajima	SEL 203	5934

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
10/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	09/635,945	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-28,30-50 and 67-94* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-28,30-50 and 67-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/27/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-28, 30-50 and 67-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US 5,825,449) in view of Taguchi (Taguchi et al., US 6,121,632) and/or Kwasnick (Kwasnick et al., US 5,198,694; of record).

Shin discloses a semiconductor device (Figs. 1a-1f; also see col. 1, lines 34-67; a liquid crystal display device), comprising: a substrate (1; glass); a thin film transistor comprising a gate electrode (2), a first insulating layer over the gate electrode, a channel forming region in a first semiconductor layer (4), and doped source and drain regions in a second semiconductor layer (5); a second interlayer insulating layer (9; nitride, inorganic); a pixel electrode (6); a storage capacitor wiring ("20" and/or "2D"); and, a source input terminal portion (a source pad, also see the top row pads 640 in Fig. 6) including a first layer (2A) comprising the same material as that of the gate electrode (2) and a second layer (6A) comprising the same material as that of the pixel electrode in contact with the first layer through a contact hole formed only in the first insulating layer, wherein the gate electrode, the storage capacitor wiring layer and the first layer in the input terminal portion all have a tapered portion and are formed from a same

conductive layer; and the storage capacitor wiring and a portion of the pixel electrode, with a portion of the first insulating layer disposed therebetween, inherently form a storage capacitor. The device further comprises a source (or first) wiring (7; also see source wiring 610 in Fig. 6), wherein a portion of the wiring (7) is formed over the source region (left side of film 5) and another portion of the source wiring (7) is formed on the second layer (6A) of the source input terminal portion. And, it is also noted that the second insulating layer (9) in Shin can be regarded as being naturally overlapping with the pixel electrode (6), as the second insulating layer (9) therein overlaps with at least a portion of the pixel electrode (6).

Shin does not expressly disclose that the channel formation region (i.e., the first portion) of the first semiconductor layer can have a thickness thinner than that of the rest of the first semiconductor layer. However, one of ordinary skill in the art would readily recognize that such thinner portion can be desirably formed through over etching of the overlying heavily doped source/drain layer (i.e., the second semiconductor layer) so as to prevent any potential shorting from happening by any residuals of the overlying heavily doped source/drain layer, as evidenced in Taguchi (see the thinner portion of the channel region in layer 12 in the cover page figure) and/or Kwasnick (see the thinner portion of the channel region in layer 30 in the cover page figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to incorporate the feature of the thinner first portion in the channel formation region, such as that taught in Taguchi and/or Kwasnick, into the

device of Shin, so that a semiconductor device would be obtained with the potentially adverse electrical shorting to the channel region therein being eliminated.

Regarding claims 26-28, 30 and 35-38, it is noted that the storage wiring ("20" or "2D") in Shin can be regarded as being covered by the pixel electrode (6), as at least a portion of the storage wiring is directly covered vertically by the pixel electrode, and/or the storage wiring can be fully covered by the pixel electrode when view along certain directions/angles.

Regarding claims 39-42, although Shin and/or Hayashi do not expressly disclose that the device can be applied in one of the selected applications as recited in these claims, each of these recited application are art-known applications for an LCD device such as the one of Shin, in order to achieve better display performance with reduced size, as readily evidenced in the prior art such as Ikeda et al. (US 5,428,250; see col.1, lines 16-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device collectively taught by Shin and Hayashi, and applied it to any of the art-known applications, so that a device in any of the applications with reduced size and/or with improved display performance would be obtained.

Regarding claims 43-50, it is noted that at least a portion of the source wiring (or first wiring; 7) in Shin is covered by the second insulating layer (9) therein.

Regarding claims 67-74, it is noted that, although Shin does not expressly disclose that the gate electrode can comprise aluminum and that the pixel electrode can comprise indium, zinc and oxygen, aluminum is one of most commonly used materials

for forming the gate electrode, and In-Zn-O is one of most commonly used materials for forming the pixel electrode, as readily evidenced in the prior art such as Hayashi (US 6,094,248; see col. 5, lines 43-53; and col. 7, lines 58-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to incorporate the art-commonly-used Al-gate electrode and Ti-Zn-O pixel electrode into the device of Shin, so that a semiconductor device with desired materials and/or with improved material flexibilities for the gate and pixel electrodes would be obtained, since these materials are art-known ones that are respectively well suited for the intended uses, and it has been held that: The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 83-86, it is noted that the angle of the tapered portion in Shin is substantially between 1° and 20°, given that the lateral and vertical dimensions shown in Figs. 1a-1f of Shin are obviously in significantly different scales, as the actual lateral dimension of the TFT therein should be normally much greater than its thickness dimension, in a manner substantially same as what is shown in Fig. 8 of the instant invention. Furthermore, it is noted that the angle of the tapered portion is an art-recognized parameter of importance subject to routine experimentation and optimization.

Regarding claims 87-96, it is noted that it is well known in the art that micro-crystal semiconductor is also commonly used to form the channel forming layer in TFT,

so as to achieve the desired material choice and/or desired combination of performance and cost for the TFT, as readily evidenced in the prior art such as Iwata (US 5,144,391; see col. 1, lines 13-20) and/or Shimizu (US 5,834,345; see its abstract).

Response to Arguments

Applicant's arguments with respect to the above rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to a TFT with a micro-crystal semiconductor channel-forming layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
September 27, 2007

SHOUXIANG HU
PRIMARY EXAMINER